Reg.No.:												

VIVEKANANDHA COLLEGE OF ENGINEERING FOR WOMEN
[AUTONOMOUS INSTITUTION AFFILIATED TO ANNA UNIVERSITY, CHENNAI]
Elayampalayam – 637 205, Tiruchengode, Namakkal Dt., Tamil Nadu.

Question Paper Code: 7003

B.E. / B.Tech. DEGREE END-SEMESTER EXAMINATIONS – MAY / JUNE 2024
Sixth Semester
Electronics and Communication Engineering
U19EC625 – VLSI Design
(Regulation 2019)

Time: Three Hours Maximum: 100 Marks

Answer ALL the questions

Knowledge Levels (KL)	K1 – Remembering	K3 – Applying	K5 - Evaluating
	K2 – Understanding	K4 – Analyzing	K6 - Creating

PART – A

(10 x 2 = 20 Marks)

Q.No.	Questions	Marks	KL	CO1
1.	Why NMOS transistor is selected as pull down transistor?	2	K2	CO1
2.	What are the objectives of layout rules?	2	K2	CO1
3.	What are stick diagrams?	2	K2	CO2
4.	What are the different color codes used for single poly silicon nMOS technology?	2	K2	CO2
5.	What is the importance of pseudo-nMOS logic gates?	2	K2	CO3
6.	Draw the equivalent RC model for a two-input NAND gate.	2	K2	CO3
7.	List any two faults that occur during manufacturing.	2	K2	CO4
8.	What are the tests for I/O integrity?	2	K2	CO4
9.	What are system tasks and complier directives?	2	K2	CO5
10.	Define Module and Instance.	2	K2	CO5

PART – B

(5 x 13 = 65 Marks)

Q.No.		Questions	Marks	KL	CO
11.	a)	Explain the DC transfer characteristics of a CMOS Inverter with necessary conditions for the different regions of operation.	13	K4	CO1
		(OR)			
	b)	Develop the layout design rules and draw diagram for four input NAND and NOR gate.	13	K4	CO1
12.	a)	Compare and contrast dynamic power dissipation with static power dissipation in CMOS circuits. Discuss the techniques used to minimize each type of power dissipation and the challenges associated with their implementation.	13	K4	CO2
		(OR)			
	b)	Describe the principles behind logical effort and how it guides transistor sizing in digital circuit design. Discuss the trade-offs involved in optimizing logical effort for performance while considering power consumption.	13	K4	CO2
13.	a)	Discuss in detail about dynamic transmission gate edge triggered registers.	13	K3	CO3
		(OR)			
	b)	Classify the various Ratioed circuits for CMOS circuits and explain in detail.	13	K3	CO3
14.	a)	With neat sketch explain the CLB, IOB and programmable interconnects of an FPGA device.	13	K2	CO4
		(OR)			
	b)	Examine the boundary scan architectures and explain how to test the circuit board level and system level.	13	K2	CO4
15.	a)	Write a Verilog behavioral code for 8 to 1 MUX using CASE statement.	13	K5	CO5
		(OR)			
	b)	Explain carry look ahead adder. Write a Verilog code with data flow style program for carry look ahead adder.	13	K5	CO5

PART – C

(1 x 15 = 15 Marks)

Q.No.		Questions	Marks	KL	CO
16.	a)	Describe in detail about different types of scan design method and explain with neat diagram.	15	K3	CO4
		(OR)			
	b)	Draw and explain about Master-Slave Edge-Triggered register with its timing properties and non-ideal clock signals.	15	K4	CO3